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Power Quality Improvement Using Cascaded H-Bridge Multilevel Inverter Based Dstatcom

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Abstract
Cascaded multilevel configuration of the inverter has the advantage of its simplicity and modularity over the configurations of the diode-clamped and flying capacitor multilevel inverters. This paper presents a three-phase, five-level and seven level cascaded multilevel voltage source inverter based active filter for power line conditioning to improve power quality in the distribution network. The DSTATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL). The compensation process is based on concept of p-q theory. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package.
Keywords: DSTATCOM, Level shifted Pulse width modulation (LSPWM), Phase shifted Pulse width modulation (PSPWM), Cascaded H- Bridge Multilevel Inverter, Proportional-Integral (PI) control, CHB multilevel inverter, D-Q reference frame theory.

I. INTRODUCTION

The electric power system has grown in size and complexity with a huge number of interconnections to meet the increase in the electric power demand. Moreover, the role of long distance and large power transmission lines become more important. Now a days the requirement for power quality becomes more and more important to keep safety of the electrical devices and consumer satisfaction. Electric Power quality is a term which has captured increasing attention in power engineering in the recent years. Even though this subject has always been of interest to power engineers; it has assumed considerable interest in the 1990's. Electric power quality means different things for different people. To most electric power engineers, the term refers to a certain sufficiently high grade of electric service but beyond that there is no universal agreement [1]. The measure of power quality depends upon the needs of the equipment that is being supplied. What is good power quality for an electric motor may not be good enough for a personal computer. Usually the term power quality refers to maintaining a sinusoidal waveform of bus voltages at rated voltage and frequency. Electric power quality (EPQ) problems mainly include unbalance voltage and current, flicker, harmonics, voltage sag, dip, swell, and power interruption [2]. These power quality problems may cause abnormal operations of facilities or even trip protection devices. Hence, the maintenance and improvement of electric power quality has become an important scenario today.

The STATCOM used in distribution systems is called DSTATCOM (Distribution-STATCOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage. The D-STATCOM employs an inverter to convert the DC link voltage Vdc on the capacitor to a voltage source of adjustable magnitude and phase. Therefore the D-STATCOM can be treated as a voltage-controlled source. The D-STATCOM can also be seen as a current-controlled source.

The DSTATCOM is based on the instantaneous real-power theory; it provides good compensation characteristics in steady state as well as transient states [3]. The instantaneous real-power theory generates the reference currents required to compensate the distorted line current harmonics and reactive power. It also tries to maintain the dc-bus voltage across the capacitor constant. Another important characteristic of this real-power theory is the simplicity of the calculations, which involves only algebraic calculation

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge

(CHB), neutral point clamped, flying capacitor [4-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges.

II. DESIGN OF MULTILEVEL BASED DSTATCOM

A. Principle of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Fig-1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.
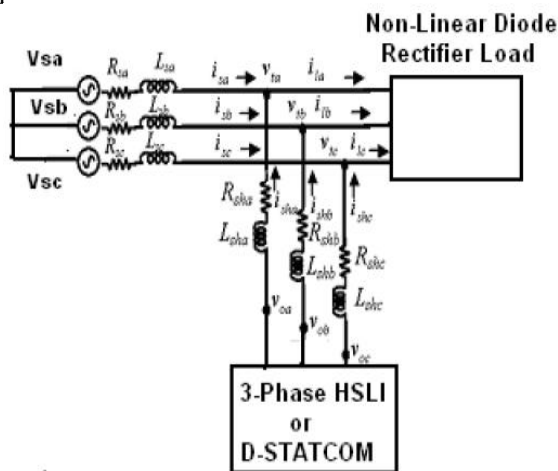

Fig.1 Schematic Diagram of a DSTATCOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes: 1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

B. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms

voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously.
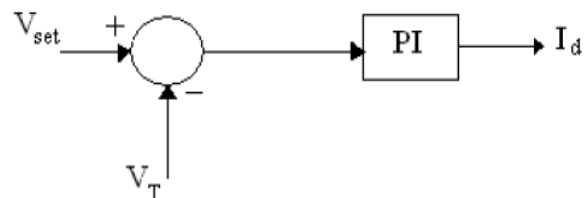

Fig-2 PI control for reactive power compensation

The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [6]. It is called the instantaneous current component (id-iq) method. This is similar to the Synchronous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V(a,b,c) and the available currents il (a,b,c) in α-β components must be calculated as given by (1), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where "θ" represents the instantaneous voltage vector angle (2).
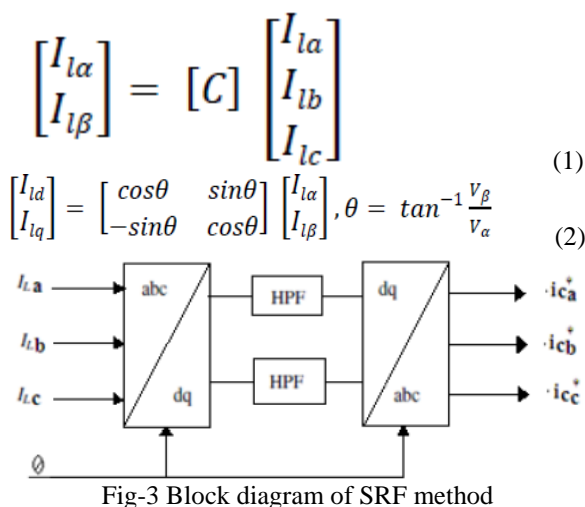
$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} I_{ld} \\ I_{lq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix}, \theta = tan^{-1}\frac{V_\beta}{V_\alpha} \tag{2}$$

Fig-3 Block diagram of SRF method

Fig. 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and un balance; therefore d θ/d t may not be constant over a mains period. With transformation given below the direct voltage component is

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \frac{1}{\sqrt{v_\alpha^2 + v_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{v_\alpha^2 + v_\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} I_{comp,a} \\ I_{comp,b} \\ I_{comp,c} \end{bmatrix} = [C]^T \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \tag{5}$$

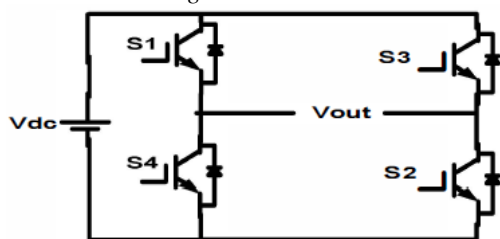*D. Cascaded H-Bridge Multilevel Inverter*

Fig-4 Circuit of the single cascaded H-Bridge Inverter

Fig4 shows the circuit model of a single CHB inverter Configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded [7]. The switching table is given in Table l.

Table-l Switching table of single CHB inverter

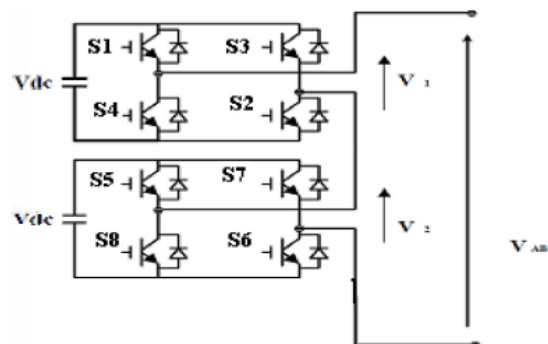| Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

Fig. 5 Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in table-2.

Table 2. Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

E. Design of Single H-Bridge Cell
1. Device Current
The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, d = l/2(1 +Kmsinωt), Where, m = modulation index K = + 1 for IGBT, -1 for Diode. For a load current given by

Iph = √2Isin (wt - ¢)   (6)

Then the device current can be written as follows.

$$\therefore i_{device} = \frac{\sqrt{2}}{2} I \sin(wt - \emptyset) x (1 + km\sin wt) \tag{7}$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} \frac{\sqrt{2}}{2} I \sin(wt - \emptyset) x (1 + km\sin wt)\, dwt$$
$$= \sqrt{2}I \left[\frac{1}{2\pi} + \frac{km}{g}\cos\varphi \right] \tag{8}$$

The device RMS current can be written as

$$i_{rms}$$

$$= \sqrt{\int_{\varphi}^{\pi+\varphi} \frac{1}{2\pi}(\sqrt{2}I \sin(wt - \emptyset))^2 \times \frac{1}{2} \times ((1 + km\sin wt)\,dwt)}$$

$$= \sqrt{2}I \sqrt{\frac{1}{g} + \frac{km}{3\pi}\cos\varphi} \qquad (9)$$

2. IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss. The conduction loss can be calculated by,

$$P_{on\,(IGBT)} = V_{ceo} * I_{avg\,(igbt)} + I^2_{rms\,(igbt)} * r_{ceo} \qquad (10)$$

$$I_{avg\,(igbt)} = \sqrt{2}I \left[\frac{1}{2\pi} + \frac{m}{g}\cos\varphi\right] \qquad (11)$$

$$I_{rms\,(igbt)} = \sqrt{2}I \sqrt{\left[\frac{1}{g} + \frac{m}{3\pi}\cos\varphi\right]} \qquad (12)$$

Values of Vceo and rceo at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig-6.
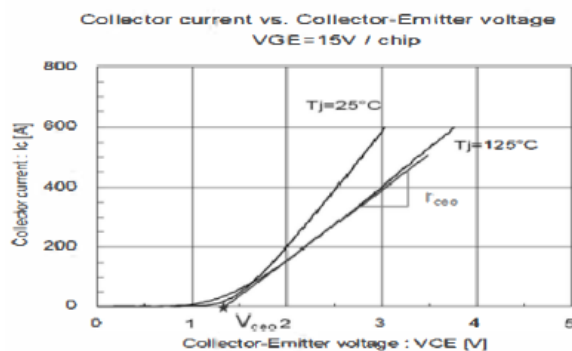
Fig. 6 IGBT output characteristics

The switching losses are the sum of all tum-on and tum-off
energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + b\bar{I} + cI^2 \qquad (13)$$

Assuming the linear dependence, switching energy

$$E_{sw} = (a + bI + cI^2) * \qquad (14)$$

Here VDC is the actual DC-Link voltage and Vnom is the DCLink Voltage at which Esw is given. Switching losses are calculated by summing up the switching energies.

$$P_{sw} = \frac{1}{T_0}\Sigma_n E_{sw}(i) \qquad (15)$$

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_0}\Sigma_n (a + bI + cI^2) = \frac{1}{T_0}\left[\frac{\bar{a}}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] \qquad (16)$$

After considering the DC-Link voltage variations, switching losses of the IGBT can be written as follows.

$$P_{sw\,(IGBT)} = f_{sw}\left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] * \frac{V_{DC}}{V_{nor}} \qquad (17)$$

So, the sum of conduction and switching losses is the total
losses given by

$$PT(IGBT) = Pon(IGBT) + Psw(IGBT) \qquad (18)$$

3. Diode Loss Calculation

The DIODE switching losses consist of its reverse recovery losses; the tum-on losses are negligible.

$$E_{rec} = a + bI + cI^2 \qquad (19)$$

$$P_{sw\,(DIODE)} = f_{sw}\left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] * \frac{V_{DC}}{V_{nor}} \qquad (20)$$

So, the sum of conduction and switching losses gives the
total DIODE looses.

$$P_{T\,(DIODE)} = P_{on\,(DIODE)} + P_{sw\,(DIODE)} \qquad (21)$$

The total loss per one switch (IGBT +DIODE) is the sum of
one IGBT and DIODE loss.

$$P_T = P_{T\,(IGBT)} + P_{sw\,(DIODE)} \qquad (22)$$

4. Thermal Calculations

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances [8] [9]. The thermal resistance equivalent circuit for a module is shown in Fig 5. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T R_{th\,(c-h)} + T_h \qquad (23)$$

Here Rth(c-h) = Thermal resistance between case and heat
Sink.

$$P_T = \text{Total Power Loss (IGBT + DIODE)} \qquad (24)$$

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j\,(IGBT)} = P_{T\,(IGBT)} R_{th\,(j-c)\,IGBT} + T_c \qquad (25)$$

The DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j\,(DIODE)} = P_{T\,(DIODE)} R_{th\,(j-c)\,DIODE} + T_c \qquad (26)$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average

junction temperature. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.
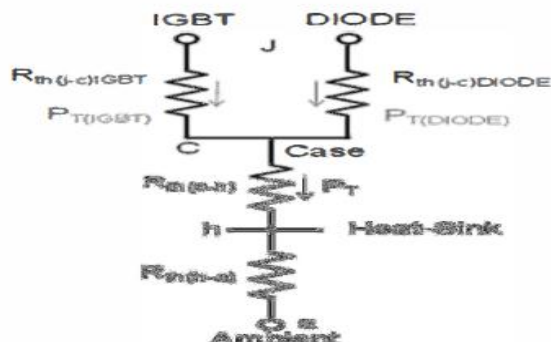

Fig. 7 Thermal resistance equivalent circuit

F. DC-Capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency.
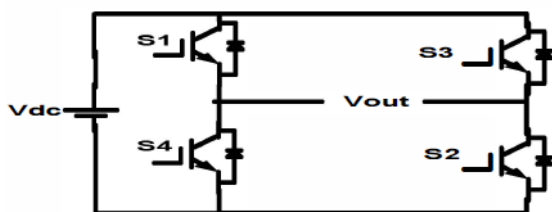

Fig.8 H-Bridge converter

$$I_c = -\frac{1}{V_{dc}}\frac{1}{2}(|U_{ac}| * k + IwL)\sin(2wt) \qquad (27)$$

Since the value of 'L' is very small, the above equation can be simplified to

$$I_c = -\frac{1}{V_{dc}}\frac{1}{2}(|U_{ac}| * k)\sin(2wt) \qquad (28)$$

$$l_c = -k\frac{1}{2}\frac{|U_{ac}|}{V_{dc}} * \sin(2wt) = -k\frac{m}{2}\sin(2wt) \qquad (29)$$

Here 'm' is the modulation index and

$$I_{cp} = C\frac{du_{pp}}{dt} ; \frac{m}{2}I\sqrt{2} = C2w*\Delta V\ V_{dc}$$

$$C = \frac{m}{4w}\frac{1}{\Delta V*V_{dc}}\sqrt{2}I \qquad (30)$$

G. PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM).

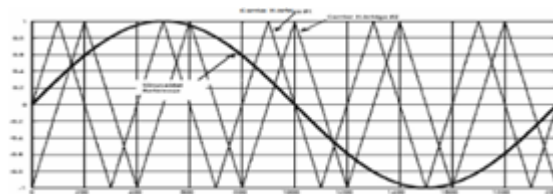*1.Phase Shifted Carrier PWM (PSCPWM)*

Fig-9 shows the Phase shifted carrier

Pulse Width Modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 1800 /m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multi level output waveform with lower distortion.

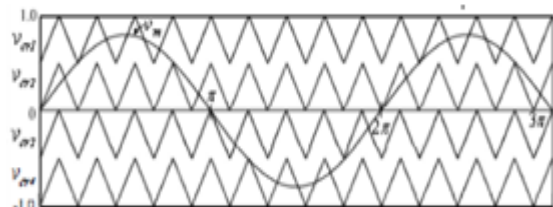*2. Level Shifted Carrier PWM (LSCPWM)*

Fig-I0 shows the Level shifted carrier

Pulse Width Modulation is nothing but, each cell is modulated independently using sinusoidal unipolar width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells [10]. A carrier Level shift by 1/m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

III. MATLAB MODELING AND SIMULATION RESULTS

The D-STATCOM model is established based on Matlab/Simulink. Here simulation is carried out in different cases such as 1) Implementation of D-Statcom using Phase Shifted Modulation Technique. 2). Implementation of D-Statcom using Level Shifted Modulation Technique.

Case 1: Implementation of D-Statcom using Phase Shifted Modulation Technique
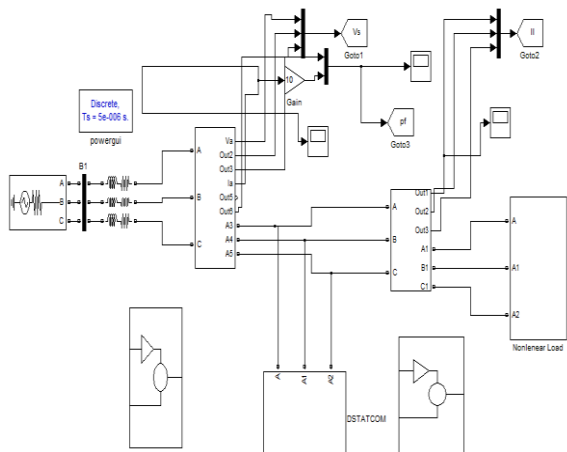
Fig.11 Matlab/Simulink Model of proposed
Compensator using Phase Shifted Modulation
Technique

Fig.11 shows the Matlab/Simulink Model of
proposed Compensator using Phase Shifted
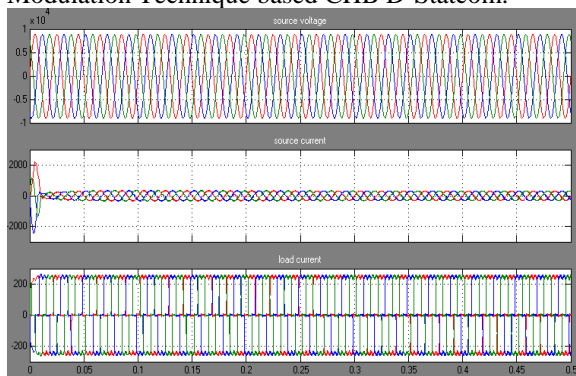Modulation Technique based CHB D-Statcom.

Fig. 10 Source Voltage, Source Current, Load
Current with Compensator

Fig.10 shows the Source Voltage, Source
Current, Load Current with Compensator, due to non-
linear diode rectifier pollutes source side current,
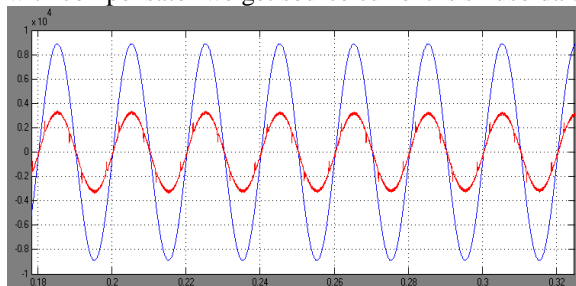with compensator we get source current is sinusoidal.

Fig. 11 Source Side Power Factor

Fig.11 shows the Source side Power Factor, both
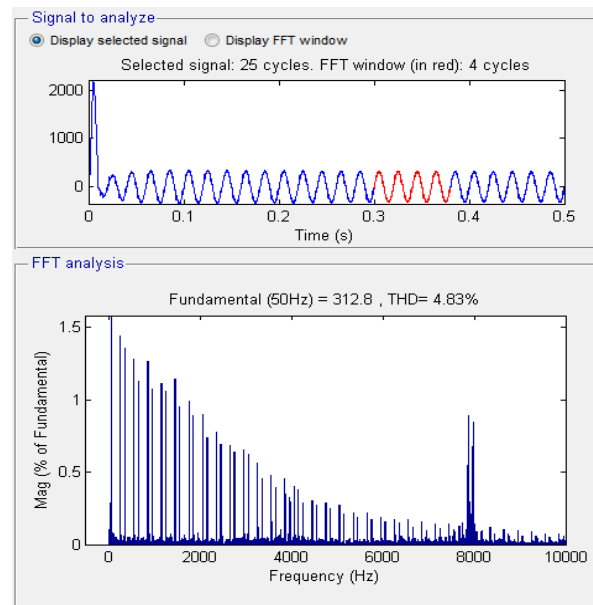voltage & current are maintained sinusoidal and in
phase condition.

Fig.12 FFT Analysis of source current with
compensator using PS Modulation Technique

Fig.12 shows the FFT Analysis of source current
with compensator using PS Modulation Technique,
we get THD is 4.83%.

*Case 2: Implementation of D-Statcom using Level
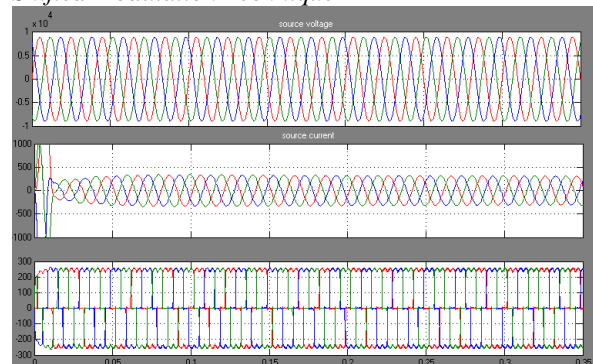Shifted Modulation Technique*

Fig. 13 Source Voltage, Source Current, Load
Current with Compensator

Fig.13 shows the Source Voltage, Source
Current, Load Current with Compensator, due to non-
linear diode rectifier pollutes source side current,
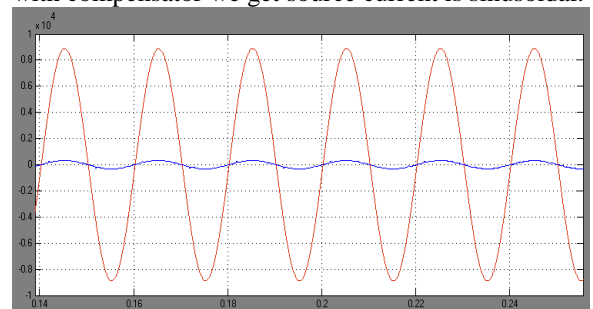with compensator we get source current is sinusoidal.

Fig.14 Source Side Power Factor

Fig.14 shows the Source side Power Factor, both voltage & current are maintained sinusoidal and in phase condition.
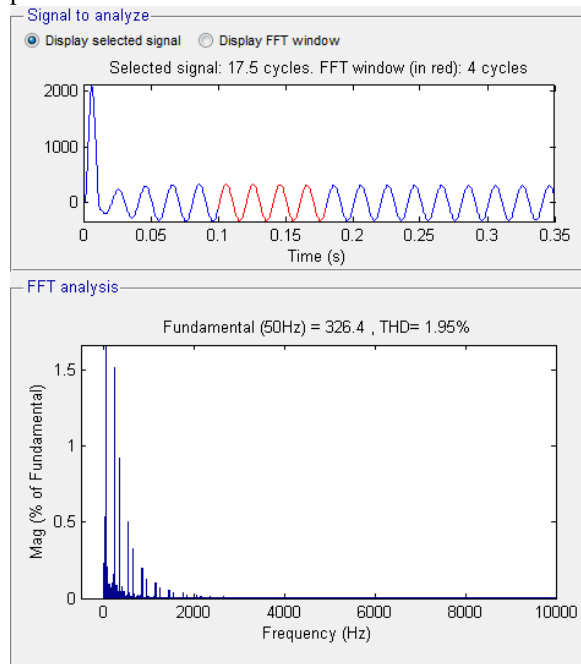

Fig.12 FFT Analysis of source current with compensator using LS Modulation Technique

Fig.12 shows the FFT Analysis of source current with compensator using LS Modulation Technique, we get THD is 1.95%.

IV. CONCLUSION

A five level cascaded multilevel voltage source inverter based DSTATCOM using instantaneous real-power controller is found to be an effective solution for power line conditioning. DSTATCOM with the proposed controller reduces harmonics and provides reactive power compensation due to non-linear load currents; as a result source current(s) become sinusoidal and unity power factor is also achieved under both transient and steady state conditions. The proposed instantaneous real-power controller uses reduced computation for reference current calculations compared to conventional approach. The cascaded inverter switching signals are generated using triangular-sampling current controller; it provides a dynamic performance under transient and steady state conditions. As evident from the simulation studies, dc bus capacitor voltage settles early and has minimal ripple because of the presence of PI-controller. The THD of the source current is investigated for both PSCPWM and LSCPWM for a five level inverter based DSTATCOM. THD simulation results under non-linear loads are investigated and found that the LSCPWM results are better than PSCPWM.

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